Low-voltage solution-processed hybrid light-emitting transistors

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Abstract

We report the development of low operating voltages in inorganic-organic hybrid light-emitting transistors (HLETs) based on solution-processed ZrO_x gate dielectric and a hybrid multilayer channel consisting of the heterojunction In_2O_3/ZnO and the organic polymer '*Super Yellow'* acting as n- and p-channel/emissive layers, respectively. Resulting HLETs operate at the lowest voltages reported to-date (<10 V) and combine high electron mobility (22 cm^2/Vs) with appreciable current on/off ratios ($\approx 10^3$) and an external quantum efficiency of 2×10^{-2} % at 700 cd/m^2. The charge injection, transport and recombination mechanisms within this HLET architecture are discussed and prospects for further performance enhancement are considered.

Keywords

Light emitting transistors; low-voltage; solution-processed organic semiconductors; hybrid transistors, metal oxide high-k dielectric

Solution processable semiconductor and dielectric materials are set to play an important role in future electronic and optoelectronic technologies due to the ability to form high quality thin films by cost-efficient, solution-based manufacturing processes[1-7]. Recently, solution-processed hybrid heterostructure (organic/inorganic) light emitting transistors (HLETs) containing an n-type metal oxide layer (acting as the electron transporting channel) and a conjugated polymer layer (acting as the light-emitting layer) have demonstrated significant potential for novel display applications[8-12]. Since HLETs provide gate controlled light emission, they can, potentially, further simplify the fabrication of display pixel devices[11,12]. However, the operating voltages for best performing HLETs have remained stubbornly high (≈100 V), hindering the demonstration of power-efficient devices. Further to high operating voltages, Si substrates, used in reported HLETs, absorb the emitted light and result in lower optical performance in comparison to similar structure organic light emitting diodes (OLEDs)[13-15] (where the metal cathode reflects light out through a transparent anode). Thus the development of low-operating-voltage HLETs incorporating solution-processed materials on non-absorbing substrates is a necessary step towards meeting the challenges for next-generation low-cost display applications. An interesting approach that can help to address this need is the use of high-k dielectric materials in combination with Al-gate electrodes in novel device architectures[16-19].

It has recently been shown that the charge carrier mobility in solution-processed metal oxide transistors can be enhanced by the introduction of low-dimensional heterostructure channel systems with carefully engineered interface energetics[1,2,17-21]. It has been argued that due to the conduction band energy offset between the two oxides employed, electrons migrate towards the hetero-interface forming a quasi-two-dimensional (2D) free-electron

system which in turn leads to remarkable improvements in the electron mobility of the device. Depending on various factors such as complexity of the heterostructure, deposition method and annealing temperature, electron mobility values up to 50 cm²/Vs have been attained[10,11]. Furthermore, it was found that the use of low temperature, solution processed and high-k dielectrics, i.e. ZrO_x (dielectric constant~25), is able to increase the charge carrier mobility of such heterostructure channel systems whilst offering a dramatic reduction in transistor operating voltage[16-18]. Similar advantages are found in using high-k ZrO_x dielectrics in ZnO and Li-doped ZnO transistors[22] and ZrO_x is also known to function effectively as an electron injection layer in hybrid light emitting diodes[23].

Herein, we report the development of low-voltage HLETs fabricated using a combination of solution-processable organic and inorganic materials with carefully selected functionalities. In particular, by integrating ultra-thin layers of the high-*k* dielectric ZrO_x with an n-channel In_2O_3/ZnO heterojunction and the p-channel highly luminescent polymer *Super Yellow* (SY), we are able to demonstrate low operating voltage (≤10 V) HLETs. Additionally, the resulting hybrid devices offer improved electroluminescence characteristics with excellent transistor operation that includes high electron mobility (≈22 $cm^2\ V^{-1}\ s^{-1}$) and appreciable ON/OFF current ratios. These attributes enable relatively high channel currents to be driven through the active layer of the HLET leading to a luminance of up to 700 cd/m^2, albeit at a modest EQE ~10^{-2} %.

The HLETs were fabricated on pre-cleaned glass substrates, employing a 50 nm-thick Al gate electrode deposited via thermal evaporation. A thin layer of native Al_2O_3 was grown by exposing the Al electrodes to ozone generated by a low-pressure mercury UV lamp. The ZrO_x precursor solution was then spin-coated on top under N_2, followed by a photochemical

curing step in ambient air (as shown in **Figure S1** in **Supporting Information**). The surface topography of each of the sequentially deposited layers was characterized using atomic force microscopy (AFM) (**Figure 1 (a-d)**). The AFM images (**Figure 1 (a-c)**) show that the thermally evaporated Al electrodes feature a relatively high root mean square surface roughness (R_{RMS}) of ~ 1.2 nm, which increases to 1.4 nm following Al_2O_3 formation. Interestingly, solution-deposition of the ZrO_x layer appears to planarize the Al/Al_2O_3 surface as evidenced by the reduced surface R_{RMS} = 0.7 nm. **Figure 1(d)** shows the corresponding surface height distributions for each sample, where the labels Al, AlOx and ZrOx refer to the top layer in the stack, i.e. the ZrOx data represents the surface of the Al/AlOx/ZrOx gate electrode/dielectric stack. **Figure 1(e)** shows the capacitance versus frequency (C-*f*) characteristics of the Al_2O_3/ZrO_x bilayer dielectrics measured in a metal/insulator/metal (MIM) configuration (see inset in **Figure 1(e)**). Analysis of the C-*f* data allows calculation of the geometrical capacitance of the gate dielectric, yielding a value of ≈235 nF/cm^2. The breakdown electric field and leakage current is shown in **Figure S2** in the **Supporting Information**.

For the n-channel, the In_2O_3 layer was subsequently grown on the dielectric by spin-coating a precursor solution (see section **Materials and Methods** in **Supporting Information**) in air followed by thermal annealing at 300 °C (also in air), repeated three times in order to increase thickness. The top ZnO layer was then deposited by spin-coating a nanoparticle solution and thermal annealing at 300 °C in air. HLET fabrication was completed using two shadow-masked evaporation steps to define complementary electron- and hole-injecting source (S) and, respectively, drain (D) contacts with an intervening emission layer deposition step resulting in a non-planar S/D geometry (**Figure 2(a)**). The electron-injecting Al S-electrode was first deposited directly on top of the In_2O_3/ZnO

heterojunction. Then a 120 nm thickness layer of the emission polymer, Super Yellow (molecular structure as shown in **Figure S3** in **Supporting Information**), [24] was spin-coated over the whole structure and annealed at 150 °C in nitrogen atmosphere. Finally, the MoO_X/Au hole-injecting D-electrode was evaporated to complete the non-planar S-D geometry[25-26]. The channel width and length of the resulting HLETs was measured to be 1 mm and 100 μm, respectively. The details of all fabrication steps are given in the section, "Materials and Methods" in **Supporting Information** and a schematic illustration of each dielectric layer and electrode deposition is depicted in **Fig. S1** and **S4 respectively** (**Supporting Information**).

Figure 2 parts **(b)** and **(c)** show the transfer and output characteristics of a representative device. The high capacitance of the Al_2O_3/ZrO_x bilayer dielectric allows these transistors to be operated at ≤10 V bias and they exhibit clear n-channel behavior with no operating hysteresis between forward and return gate voltage (V_G) sweeps for both linear and saturation regimes. An average electron mobility of ≈22 $cm^2\ V^{-1}\ s^{-1}$ was calculated from the transfer curves measured in saturation regime using the equation (1), in agreement with previous reports for similar transistor channel architectures[1-5].

$$I_{DS} = \frac{W\,C_i}{2\times L}\mu(V_{GS} - V_{TH})^2 \qquad (1)$$

where I_{DS} is the experimentally measured drain-source current, W/L is the width-to-length ratio of the device channel, V_{GS} is the operating gate voltage and C_i is the geometric capacitance of the bilayer dielectric. The electron mobility was calculated from the high voltage slope of the transfer characteristics as shown in **Figure S5** in **Supporting Information**. We further analyzed the electron mobility to calculate the reliability factor [28] of 195% and effective mobility of 43 $cm^2\ V^{-1}\ s^{-1}$ (explained and given in **Table S1** in **Supporting Information**). The device also exhibits an appreciable on/off channel current

ratio ≈5×10^2. These results represent the lowest operating voltage and highest electron mobility reported to date for a solution-processed HLET structure.

Another observation concerns the non-linear channel current (I_{DS}) increase at low drain voltage (V_{DS}) seen in **Figure 2(c)**. We attribute this to contact resistance, which although relatively low in absolute terms is nevertheless significant in the context of our high charge carrier mobility semiconductor. The contact resistance is also visible in the sigmoidal output characteristics given in **Figure S6** in **Supporting Information**. We note that further improvements should then be realizable through additional contact resistance optimization. The contact resistance from the hole injecting electrode (MoOx/Au) in inevitable in the HLETs and cannot be avoided. However, to lower the electron injection barrier into SY films from ZnO/In_2O_3 layer, a work function modifying interlayer material (e.g. Cs_2CO_3 or PEIE) can be used as reported previously[11-12].

The electrical and optical characteristics of the devices were tested within a nitrogen-filled glove box using an Agilent B2902A semiconductor parameter analyzer and a probe-station fitted with a calibrated photodiode positioned over the active region of the device according to our previously reported method[25-27]. External quantum efficiencies, EQEs, were calculated from the luminance, source-drain current and emission spectra of the devices under the assumption of Lambertian emission as reported previously[25-27] (full detail of electrical and optical characterization is given in **Supporting Information**). **Figure 3(a)** shows the current density and luminance plotted as a function of the applied gate voltage. Current density here (mA-A/cm^2) is calculated from the field-effect channel current density (A-kA/cm^2) taking into account the observation that the current contributing to emission is spread over the entire recombination zone area (width 12 μm x length 2 mm) rather than

being confined only to the charge accumulation layer as described earlier [8-12,29]. At V_{DS} = 10 V and V_{GS} = 10 V we find J = 2 A/cm^2. **Figure 3(b)** reports the external quantum efficiency, EQE, (%) as a function of luminance (cd/m^2) for a typical HLET; the inset shows an optical micrograph of the HLET channel during operation with visible light-emission emanating from close to the MoO_X/Au D-electrode. This suggests that unbalanced injection/transport is playing a key role with an excess of electrons accumulating in the channel and injected into the SY film close to the D-electrode. A maximum luminance of 700 cd/m^2 is achieved at the highest investigated drain current (2 A/cm^2) and gate voltage (10 V). An interesting feature is the observed saturation of the calculated EQE at a maximum value close to 2×10^{-2} %. The latter value is similar to that reported previously for HLETs operated at significantly higher gate voltages (≈ 100 V).[8-11] The light emission zone also did not shift with S-D voltage appearing stationary at the hole-injecting electrode, again characteristic of unipolar, or heavily unbalanced charge transport. The optical micrograph of the working device shown in the inset to **Figure 3b** was further analyzed (**Figure S7, Supporting Information)**, yielding an emission zone width of 12(±2) μm. The electroluminescence (EL) and photoluminescence (PL) spectra of the HLET are shown in **Figure 4(a)** and accord with the expected emission from SY[24-26]. EL was recorded for V_{DS} = 10 V, V_G = 10 V and J_{DS} = 2 A/cm^2 and PL under optical excitation at 365 nm using a LED source. We note that since the MoO_x/Au D-electrode is not fully transparent (**Figure S8, Supporting Information)**, the observed light is most likely limited to photons emitted from around the edges of the electrode, with additional exciton generation and emission expected to occur beneath it. This will lead to an underestimate of the emission efficiency, in agreement with previous reports[8,11,26]. However, it is worth mentioning that the HLET architecture employing the Al bottom-gate electrode exhibit higher EQE than previously reported HLETs fabricated on Si^{++} substrates[8]. We attribute this to reflection of the emitted light by the bottom Al gate through the

semitransparent top drain electrode. The overall result is an increase in the measured EQE. In contrast, most of the previously reported HLETs were fabricated on Si^{++} substrates where a fraction of the emitted photons are absorbed by the Si^{++}, resulting in a lower EQE.[8-12] The advantages of the proposed HLET architecture over previously reported HLETs are summarized in **Table S2** in the **Supporting Information**.

HLET operation therefore involves the following four steps; (i) electron injection from the Al S-electrode into the 3.8 - 4.0 eV [18] conduction band of the In_2O_3/ZnO heterostructure, (ii) transport of electrons along the In_2O_3/ZnO interface, (iii) accumulation of electrons at the interface between In_2O_3/ZnO and SY, and (iv) recombination of these electrons with holes injected from the MoO_x/Au D-electrode into the highest occupied molecular orbital (HOMO) of SY (5.3 eV).[25-26]. From the schematic energy level diagram in **Figure 4(b)** and the above discussion it seems likely that an electron injection interlayer could be used to help overcome the large electron injection barrier between the conduction band of In_2O_3/ZnO and the lowest unoccupied molecular orbital (LUMO) of Super Yellow[25-26] and that this should lead to higher efficiency and a more uniform emission zone. Further studies will address this consideration.

In summary, low operating voltage hybrid light-emitting transistors were successfully demonstrated using a stack channel architecture composed of a solution-processed metal oxide dielectric, a solution-processed heterojunction metal oxide n-channel and a conjugated light-emitting polymer. Resulting devices exhibit clear n-channel transistor characteristics with a high electron mobility of ≈22 cm^2/Vs. Under normal operating conditions, the devices emit bright yellow light, characteristic of the SY polymer used. Quantitative analysis of the light-emission yields a device luminance of up to 700 cd/m^2 at a maximum EQE of 2×10^{-2} %.

These are the lowest-operating-voltage HLETs reported to date and highlight the potential of our multilayer hybrid channel architecture.

Supporting Information:

Materials and Methods, Device fabrication: dielectrics layers deposition, Breakdown electric filed for the dielectric stack and device leakage current, Chemical structure of the emissive polymer PD-132, "Super Yellow", Device fabrication: electrodes and emissive layer deposition, Reliability factor and effective mobility calculation, Linear fit to the SQRT (IDS) vs. VGS and effective mobility, Electrical and optical output characteristics, Microscopic image intensity profile of the HLET channel and electrodes, Transmission of hole injecting MoOx/Au electrode, Comparison of charge carrier mobilities and operating voltages in HLETs.

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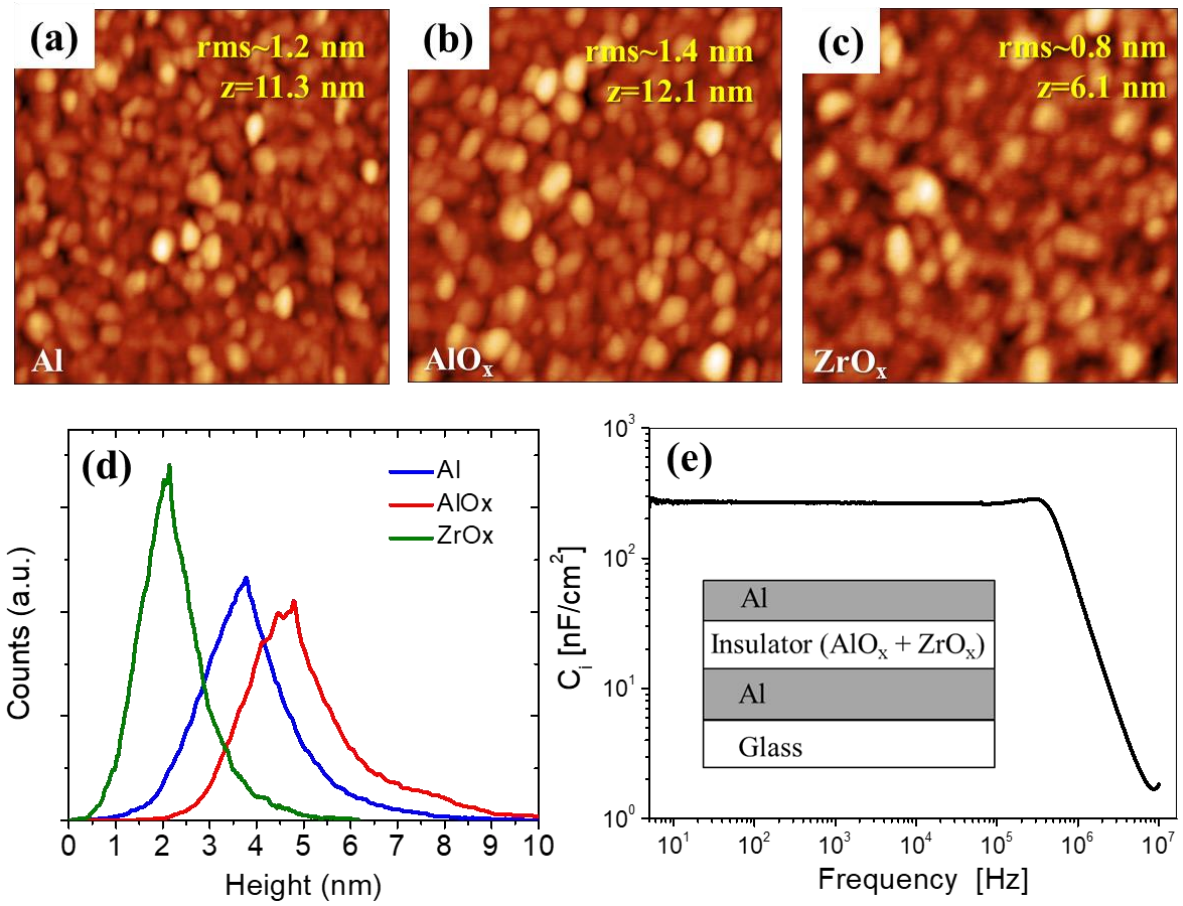

Figure 1. Sequential atomic force micrograph images (1µm x 1µm) of the top surface of **(a)** Al, **(b)** Al/AlO_x, **(c)** Al/AlO_x/ZrO_x layers and **(d)** height distributions for these images. **(e)** Capacitance *vs* frequency characteristics of the solution processed AlOx/ZrO_x bilayer dielectrics; the inset shows the metal/insulator/metal device structure used for capacitance measurements.

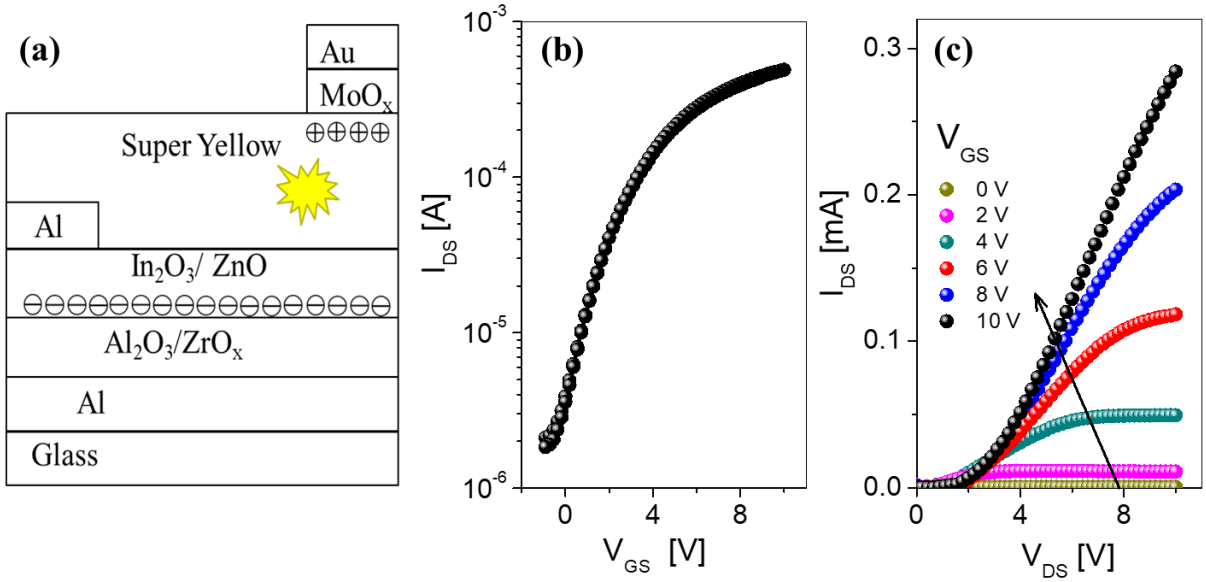

Figure 2. **(a)** Schematic HLET device structure comprised of light emitting polymer and solution processed dielectric and charge transport layers. **(b)** Electrical transfer and **(c)** Output characteristics of a HLET device.

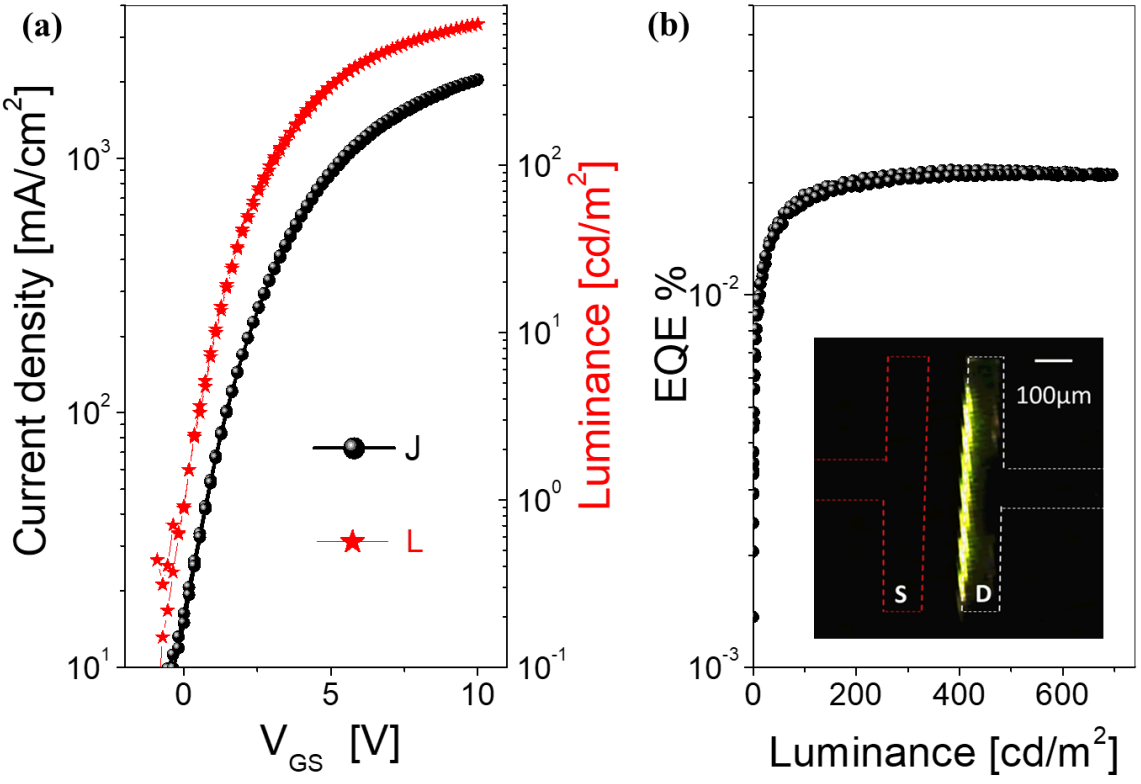

Figure 3. (a) Current density (J) and Luminance (L) as function of gate voltage. (b) External quantum efficiency of the HLET as a function of luminance; the inset shows an optical micrograph of the light emission emanating from the channel. The geometry of the buried source electrode is illustrated by the red dashed line.

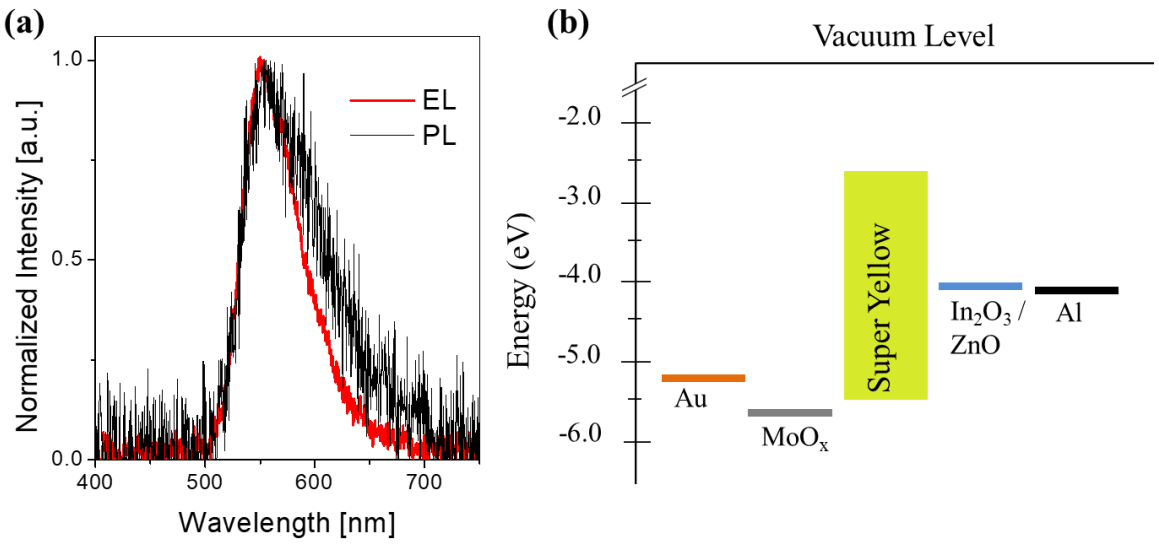

Figure 4. (a) Normalized photoluminescence (PL) and electroluminescence (EL) spectra for the HLET under optical and electrical excitation. (b) Schematic Energy level diagram for the materials used in the HLETs.

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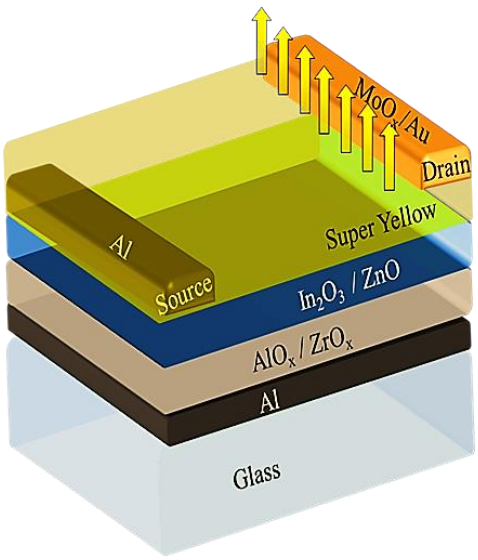
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